REMARKS

With this Response, claims 2 and 17 are amended. Applicant respectfully requests that claims 3 and 18 be canceled without prejudice. Therefore, claims 2, 4-17, and 19-31 are pending.

Claim Rejections - 35 U.S.C. § 103

Grisamore Reference

Claims 2-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,535,901 issued to Grisamore (*Grisamore*). Claims 3 and 18 have been canceled; therefore, rejection of these claims is moot. Applicant submits that the reference does not render obvious the invention as recited in the remaining claims for at least the following reasons.

Claim 2 as amended recites the following:

> **analyzing input terms on a bit-wise basis** to segment each level of bit significance of the input terms;
> selecting resources to generate a summing module based, at least in part, on the analysis; and
> designing a hyperpipelined series of Boolean function generators to implement a Wallace-architecture of full-adders, half-adders, and associated registers in the selected resources, the series of Boolean function generators to combine the input terms to produce intermediate summation results.

Claim 17 similarly recites analyzing input terms on a bit-wise basis.

The Office Action asserts at page 2 that *Grisamore* discloses a Wallace-architecture that "clearly depends on a bit-wise analysis of the input terms within each level of bit-significance." Applicant notes that the Office Action fails to provide any reasoning, or support from the cited reference for this assertion. Applicant is unable to determine from the Office Action or the reference where the reference is purported to clearly disclose or even suggest a bit-wise analysis of the input terms. Rather *Grisamore* discloses that its Wallace-architecture is based, not on a bit-wise analysis of the input terms, but upon "one of [a] plurality of reduction patterns and the

size of the current partial products." Col. 2, lines 35 to 41. Specifically, *Grisamore* at col. 2, lines 29 to 41 states:

> The method and apparatus includes processing that begins by **determining number of current partial products** for a multiplication of a first multiplicand and a second multiplicand. The processing then continues by **determining size of the current partial products**. The processing then continues by **identifying one of a plurality of reduction patterns based on the size** of the current partial products. The processing then continues by determining number of, and configuration of, full adders and half adders required for a reduction function of the current partial products **based on the one of the plurality of reduction patterns and the size** of the current partial products, wherein the multiply-accumulator performs the reduction function.

Grisamore describes this process in detail at col. 7, line 30 to col. 8, line 37, with a detailed description of Figure 9. Importantly, *Grisamore* in every case describes the processing of the input terms in reference to the size of the input terms. A preselected pattern is identified based on the size of the input terms, and the pattern is used to generate *Grisamore*'s reduction circuit. At col. 8, lines 9 to 11, *Grisamore* states: "as one of average skill in the art will appreciate, each row of reduction will have a **specific pattern** of full adders and half adders **based on the width of the row**." *Grisamore* then discusses, et seq., how the specific patterns for the reduction levels are obtained. Noticeably, *Grisamore* fails to disclose or suggest analyzing the input terms on a bit-wise basis and selecting resources to generate a summing module based on the analysis, as recited in the claims. Thus, Applicant respectfully submits that the cited reference fails to provide support for the assertion in the Office Action. For at least this reason, Applicant submits that a prima facie case of obviousness under MPEP § 2143 has not been established. Therefore, the invention as recited in claims 2 and 17 is nonobvious over the cited reference.

Furthermore, MPEP § 2143.03 sets forth that if an independent claim is nonobvious, any claim depending from the independent claim is also nonobvious. Because claims 4-16 and 19-31

depend, respectively, from claims 2 and 17, Applicant submits that these claims are also nonobvious.

Costa Reference

Claims 2-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,935,201 issued to Costa et al. (*Costa*). Claims 3 and 18 have been canceled; therefore, rejection of these claims is moot. Applicant submits that the reference does not render obvious the invention as recited in the remaining claims for at least the following reasons.

As set forth above, claim 2 as amended recites in part:

> **analyzing input terms on a bit-wise basis to segment each level of bit significance of the input terms;**

Claim 17 similarly recites analyzing input terms on a bit-wise basis to segment each level of bit significance.

The Office Action asserts at page 3 that *Costa* discloses a Wallace-architecture that "clearly depends on a bit-wise analysis of the input terms within each level of bit-significance." Applicant notes that the Office Action fails to provide any reasoning, or support from the cited reference for this assertion. The Office Action merely points to figures 7-9 as supporting what is asserted. Applicant is unable to determine from the Office Action or the reference where the reference is purported to clearly disclose or even suggest a bit-wise analysis of the input terms within each level of bit-significance. Rather than disclosing what is claimed, Applicant notes that *Costa* is noticeably silent on segmenting input terms within each level of bit significance. *Costa* fails to disclose or suggest that a level of bit significance is considered in determining the design of *Costa*'s multiplier, in contrast to what is recited in claims 2 and 17. Thus, *Costa* fails to disclose or suggest at least this element of the claims. At least because every element of the claimed invention is not found in the cited reference, Applicant submits that a prima facie case of

obviousness under MPEP § 2143 has not been established. Therefore, the invention as recited in claims 2 and 17 is nonobvious over the cited reference.

Furthermore, MPEP § 2143.03 sets forth that if an independent claim is nonobvious, any claim depending from the independent claim is also nonobvious. Because claims 4-16 and 19-31 depend, respectively, from claims 2 and 17, Applicant submits that these claims are also nonobvious.

Conclusion

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, all pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

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Gregory D. Caldwell
Reg. No. 39,926

12400 Wilshire Blvd., 7th Floor
Los Angeles, CA 90025-1026
Telephone: (503) 684-6200

GDC/VHA